Sussex Research Online

Charge trapping mechanism leading to sub-60-mV/decade-Swing FETs

Article (Accepted Version)

Daus, Alwin, Vogt, Christian, Munzenrieder, Niko, Petti, Luisa, Knobelspies, Stefan, Cantarella, Giuseppe, Luisier, Mathieu, Salvatore, Giovanni A and Troster, Gerhard (2017) Charge trapping mechanism leading to sub-60-mV/decade-Swing FETs. IEEE Transactions on Electron Devices, 64 (7). pp. 2789-2796. ISSN 0018-9383

This version is available from Sussex Research Online: http://sro.sussex.ac.uk/id/eprint/68771/

This document is made available in accordance with publisher policies and may differ from the published version or from the version of record. If you wish to cite this item you are advised to consult the publisher's version. Please see the URL above for details on accessing the published version.

Copyright and reuse:
Sussex Research Online is a digital repository of the research output of the University.

Copyright and all moral rights to the version of the paper presented here belong to the individual author(s) and/or other copyright owners. To the extent reasonable and practicable, the material made available in SRO has been checked for eligibility before being made available.

Copies of full text items generally can be reproduced, displayed or performed and given to third parties in any format or medium for personal research or study, educational, or not-for-profit purposes without prior permission or charge, provided that the authors, title and full bibliographic details are credited, a hyperlink and/or URL is given for the original metadata page and the content is not changed in any way.

http://sro.sussex.ac.uk

Charge trapping mechanism leading to Sub-60 mV/dec-Swing Field-Effect Transistors

Alwin Daus, Christian Vogt, *Student Member, IEEE,* Niko Münzenrieder, *Member, IEEE,* Luisa Petti, *Member, IEEE,* Stefan Knobelspies, Giuseppe Cantarella, Mathieu Luisier, Giovanni A. Salvatore, and Gerhard Tröster, *Senior Member, IEEE*

***Abstract*—In this work, we present a novel method to reduce the subthreshold swing of field-effect transistors below 60 mV/dec. Through modeling, we directly relate trap charge movement between the gate electrode and the gate dielectric to subthreshold swing reduction. We experimentally investigate the impact of charge exchange between a Cu gate electrode and a 5 nm thick amorphous Al_2O_3 gate dielectric in an $InGaZnO_4$ thin-film transistor. Positive trap charges are generated inside the gate dielectric while the semiconductor is in accumulation. During the subsequent de-trapping, the subthreshold swing diminishes to a minimum value of 46 mV/dec at room temperature. Furthermore, we relate the charge trapping/de-trapping effects to a negative capacitance behavior of the Cu/Al_2O_3 metal-insulator structure.**

***Index Terms*—Subthreshold swing (SS), field-effect transistor (FET), charge trapping, negative capacitance (NC), thin-films.**

I. Introduction

RECENTLY, novel paths for steep subthreshold swing (SS) devices have received increased attention due to the need for lower power dissipation and higher energy efficiency in modern electronics. One of the main reasons has been the approach of intrinsic physical limits in conventional field-effect transistors (FETs), whose SS cannot be reduced below 60 mV/dec at room temperature [1]. This inherent scaling limit has triggered the investigation of various alternative device technologies and principles. The alteration of the channel conduction mechanism has been facilitated in tunnel-FETs [2], [3] and impact-ionization-FETs [4]. Other approaches target gate-amplification in suspended-gate structures [5], [6] or with ferroelectric materials [7]–[9]. The latter ones have particularly been known as negative capacitance (NC) devices [6], [7].

NC has been observed in a variety of physical systems since the 1970's [10]–[12]. Until today, NC has been reported in e.g. electrochemical systems (batteries [10]), optoelectronics (e.g. light-emitting diodes [13]–[15] and laser diodes [13]) as well as electronic devices (e.g. FETs [16] and Schottky diodes [17]–[19]). In most cases, the phenomenon has been observed in the presence of traps for a wide range of materials such as silicon [20], [21], III-V semiconductors [13], [16], [18], [22], [23] and organic semiconductors [14], [15], [24]. Since Salahuddin [7] proposed the application of NC for steep SS FETs, ferroelectric materials have been subject of a number of reports showing their NC properties [25]–[27]. However, the other abovementioned materials and underlying physical phenomena, exhibiting NC, have so far not become popular in the race for steep SS devices.

Up to now, charge trapping has been avoided when aiming for an improved SS as it typically deteriorates FET switching [28], [29]. Nevertheless, recent work proposed charge trapping from the gate electrode as an approach to increase the gate capacitance leading to an increased drain current I_D [30]. Similarly, charge exchange between the gate electrode and a floating gate metal embedded into the gate stack has been lately investigated for a reduction of the operating voltage [31]. In this work, we evaluate a new approach by demonstrating that charge trapping can be used as a tool to decrease the SS. Through modeling, we demonstrate how the gate electrode-dielectric charge exchange rate can cause effective switching amplification. Our experimental validation shows a minimum SS of 46 mV/dec at room temperature for charge de-trapping, thus delivering the desired break-through of the 60 mV/dec-limit. Furthermore, we experimentally confirm that NC behavior can be observed in our constituted material stack. Our work provides a starting point for the investigation of novel avenues for steep SS devices.

II. Device Concept and Architecture

In this section, the basic device concept for the theoretical modeling and the experimentally realized device architecture are presented. The device concept is based on charge exchange between the gate electrode and the gate dielectric (see Fig. 1(a)). The charge exchange requires trap states within the gate dielectric (shown in light blue) which can be filled or emptied by adjusting the gate metal's Fermi level. The formation of trap charge inside the gate dielectric leads to a trap charge voltage V_{Ch}, which has a capacitive interaction with the semiconductor channel via the gate dielectric. The energy position of the gate metal's Fermi level can be controlled by the externally applied gate-source voltage V_{GS}. Hence, V_{Ch} is a function of V_{GS}. The gate current I_G is used to monitor the trap charge movement from the gate side into

A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, G. A. Salvatore and G. Tröster are with the Electronics Laboratory, ETH Zürich, Zürich, 8092, Switzerland, (e-mail: dausa@ife.ee.ethz.ch; christian.vogt@ife.ee.ethz.ch; niko.muenzenrieder@ife.ee.ethz.ch; luisa.petti@ife.ee.ethz.ch; stefan.knobelspies@ife.ee.ethz.ch; giuseppe.cantarella@ife.ee.ethz.ch; giovanni.salvatore@ife.ee.ethz.ch; troester@ife.ee.ethz.ch).

N. Münzenrieder is with the Sensor Technology Research Center, Department of Engineering and Design, University of Sussex, Richmond 3A07, Brighton, UK (e-mail: N.S.Munzenrieder@sussex.ac.uk).

M. Luisier is with the Integrated Systems Laboratory, ETH Zürich, Zürich, 8092, Switzerland, (e-mail: mluisier@iis.ee.ethz.ch).

Manuscript received January 25, 2017

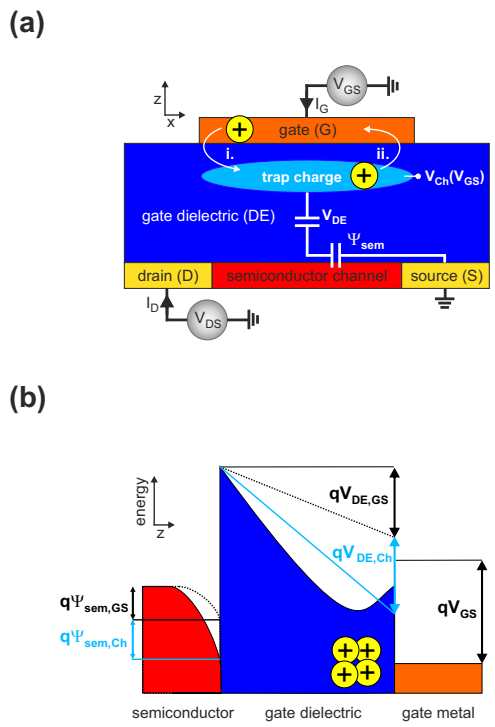

Fig. 1. Device concept. (a) The schematic illustrates the charge exchange between the gate electrode and the gate dielectric resulting in a trap charge and a trap charge voltage V_{Ch}. (b) The corresponding band diagram displays the effect of the gate-source voltage V_{GS} on the gate dielectric and semiconductor in dashed lines. The effect of a positive V_{Ch} causes additional band bending for the gate dielectric and semiconductor. For the modeling, the linearized simplification marked in light blue is assumed.

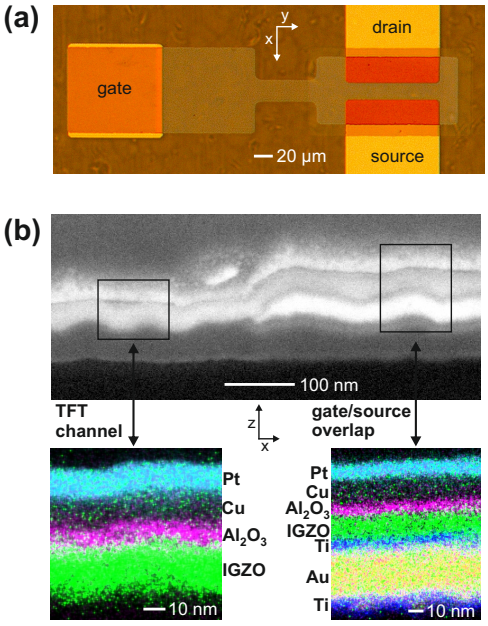

Fig. 2. Experimentally realized thin-film transistor (TFT). (a) Optical micrograph of a thin-film transistor with a channel width of 100 μm and a channel length of 20 μm. (b) Cross section of a thin-film transistor (TFT). Top: scanning-electron micrograph (SEM), bottom: energy-dispersive x-ray spectroscopy (EDX) element mapping superimposed on transmission-electron micrographs (TEM). Source/drain electrodes, semiconductor, gate dielectric and gate electrode are Ti/Au/Ti, IGZO, Al_2O_3 and Cu, respectively. The Pt coating was applied prior to SEM imaging.

the dielectric. The band diagram of the gate stack at positive V_{GS} is displayed in Fig. 1(b). The situation without any trap charge is represented by the dashed black lines showing band bending in the semiconductor (accumulation) and the voltage drop over the gate dielectric. The existence of positive trap charge causes then additional semiconductor band bending and a non-linear down-bending of the gate dielectric. The non-linearity is caused by the finite distance of the trap charge from the gate electrode and its spacial distribution. For simplicity, we assume for the modeling that the gate dielectric band shift is linear and V_{Ch} is located at the interface between the gate dielectric and the gate metal (light blue).

In Fig. 2, the experimental device architecture, which leads to the constituted device concept, is introduced. The gate dielectric with intrinsic trap states is realized by low-temperature atomic-layer deposition (ALD) of Al_2O_3. An optical micrograph of an experimentally realized thin-film transistor (TFT) is shown in Fig. 2(a). The device is fabricated on a free-standing 50 μm thick polyimide foil as described in [32]. Fig. 2(b) displays the cross-section of a TFT in a scanning-electron microscope (SEM) image and in a transmission-electron microscope (TEM) image superimposed with an element mapping by energy-dispersive x-ray spectroscopy (EDX). The semiconductor consists of 15 nm thick $InGaZnO_4$ (IGZO) [33] and the Al_2O_3 gate dielectric is 5 nm thick. The gate electrode is formed by 20 nm thick Cu. For the source/drain electrodes, Ti/Au/Ti (5/30/5 nm) is used.

III. Electrical Characteristics

The transfer characteristic of a TFT at two different maximum gate-source voltages $V_{GS,max}$ is presented in Fig. 3(a). The characteristics at $V_{GS,max} = 1$ V and $V_{GS,max} = 2$ V have been acquired at sweep rates of 5.5 mV/s and 11 mV/s, respectively. We also investigated faster sweep rates up to 1600 mV/s and found similar behavior compared to the results that are presented here. The TFT shows a counter-clockwise hysteresis in I_D, which indicates a positive charge trapping when V_{GS} is positive. I_G exhibits an increase due to channel electron tunneling through the gate dielectric (i.). In the back sweep, I_G has a peak around $V_{GS} = 0$ V, which represents the de-trapping of the positive charge (ii.). The forward sweep SS is not significantly influenced by charge trapping showing a minimum value of >80 mV/dec, whereas the minimum back sweep SS is strongly reduced yielding 54 mV/dec and 46 mV/dec for $V_{GS,max} = 1$ V and $V_{GS,max} = 2$ V, respectively (Fig. 3(b)). The reduction of the SS is caused by simultaneous de-trapping of the positive charge and the semiconductor transition from accumulation to depletion. The material parameters, such as gate dielectric thickness and gate electrode material, influencing the charge trapping/de-trapping behavior and related device physics are investigated in detail in [32]. The output characteristic of the TFT is displayed in Fig. 3(c) with typical linear and saturation regimes. The slight I_D reduction at $V_{GS} = 2$ V and $V_{DS} > 2$ V can be attributed to de-trapping on the drain side as the gate-drain voltage V_{GD} reaches values down to -0.5 V.

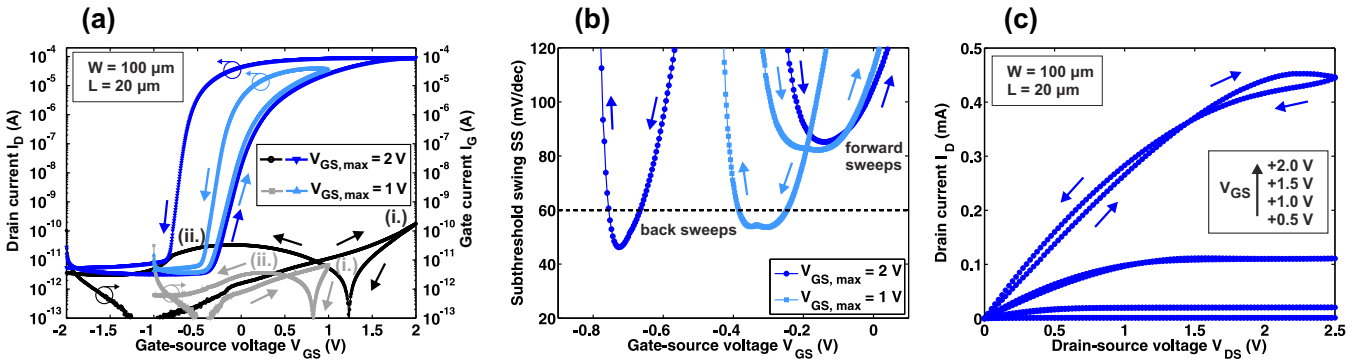

Fig. 3. Electrical characteristics of an experimentally realized thin-film transistor (TFT). (a) Transfer characteristic of a TFT for two different maximum gate-source voltages $V_{GS,max}$, where (i) indicates the channel electron tunneling gate current (I_G) generating positive charge and (ii) indicates the de-trapping I_G. (b) Subthreshold swing SS of the device shown in (a). The back sweep SS is reduced from simultaneous de-trapping of the positive charge. (c) Output characteristic of the TFT.

IV. Modeling

The modeling section is divided into the fitting of the experimental data (*A.*) and the theoretical modeling of SS (*B.*). For that purpose, it is assumed that V_{Ch} impacts I_D through a capacitive coupling to the semiconductor surface potential Ψ_{sem} and that V_{Ch} acts as a V_{GS}-controlled voltage source at the gate in superposition with V_{GS}.

A. Fitting of the experimental data

The de-trapping by resonant tunneling reveals the trap charge energy distribution where the current peak represents the energy center of the trap charge [34]. Its relation to V_{GS} (i.e. the gate metal's Fermi energy) can be used to assess the impact of the changing trap charge on the TFT switching characteristics. The de-trapping of the trap charge as a function of V_{GS} is weighted by computing the integral of the negative back sweep I_G (green) over V_{GS}, yielding the de-trapping function $F(V_{GS})$ (red) (see Fig. 4). A relative measure for the amount of trap charge can then be approximated by $\gamma(V_{GS}) = (1\text{-}F/F_{max})$, where F_{max} is the maximum value of F (in this example at $V_{GS} = -2$ V). Hence, γ is a normalized version of F, where initially $\gamma = 1$, and finally $\gamma = 0$ after the de-trapping is completed.

The flow chart in Fig. 5 represents the functional sequence of the fitting procedure. The abovementioned determination of the fitting function is represented in steps 1 and 2.

The impact of the capacitively coupled trap charge on the semiconductor channel can be described by the voltage V_{Ch}, which is justifiable as the charge is proportional to the voltage in a capacitor ($Q_{Ch} = C_{Ch} \cdot V_{Ch}$). The use of V_{Ch} facilitates the superposition with V_{GS} and enables fitting without the exact knowledge of the amount of charge Q_{Ch} or its distance from the semiconductor channel (which is embedded in the trap charge capacitance C_{Ch}). Thus, the relative change of V_{Ch} is described by $V_{Ch}(V_{GS}) = \gamma(V_{GS}) \cdot V_{Ch,max}$, where the maximum amount of trap charge is represented by the maximum trap charge voltage $V_{Ch,max}$ (step 3). $V_{Ch,max}$ is used as a fitting parameter. It is assumed that the I_D of the V_{GS} forward sweep is negligibly influenced by charge trapping and thus it is regarded as a reference for the fitting procedure.

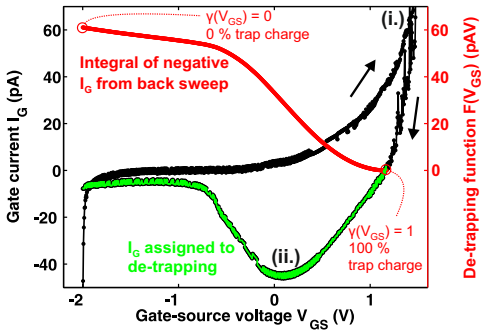

Fig. 4. Gate current I_G in a thin-film transistor. (i.) and (ii.) denote the positive charge trapping and de-trapping, respectively. The negative I_G peak represents the charge energy distribution in the gate dielectric [34]. The integral of I_G yields the de-trapping function $F(V_{GS})$. The fitting factor $\gamma(V_{GS})$ is defined by the normalized integral in the form of $\gamma(V_{GS}) = (1\text{-}F/F_{max})$. The application of $\gamma(V_{GS})$ for the fitting is described in Fig. 5.

The fitting approach directly relates the forward sweep I_D to the back sweep I_D thereby utilizing the extracted de-trapping function (i. e. γ). The superposition of V_{Ch} and V_{GS} is realized by applying V_{Ch} as a shift of the reference (forward) I_D on the V_{GS} axis (step 4). $V_{Ch,max}$ is iteratively changed until the fit (shifted forward sweep I_D) and the experimental back sweep I_D agree with each other (steps 5 and 3*). Finally, the SS of the fit and the experimental data are compared (step 6). An exemplary final fitting result for I_D is reported in Fig. 6, while Fig. 7 shows $V_{Ch,max}$ and the static threshold voltage shift ΔV_{Th} as a function of $V_{GS,max}$. The rise of both quantities demonstrates increased charge trapping for higher $V_{GS,max}$, which is caused by an increased tunneling I_G for higher positive V_{GS} [32].

B. Theoretical modeling of the subthreshold swing (SS)

In accordance with Fig. 1(b), we assume that the trap charges generate V_{Ch} which acts on Ψ_{sem} in superposition with V_{GS}. The introduction of V_{Ch} into the system leads to the following relationship for the voltages in the MOS structure:

$$V_{GS} + V_{Ch}(V_{GS}) = \Psi_{sem} + V_{DE}(\Psi_{sem}) + V_{FB}, \qquad (1)$$

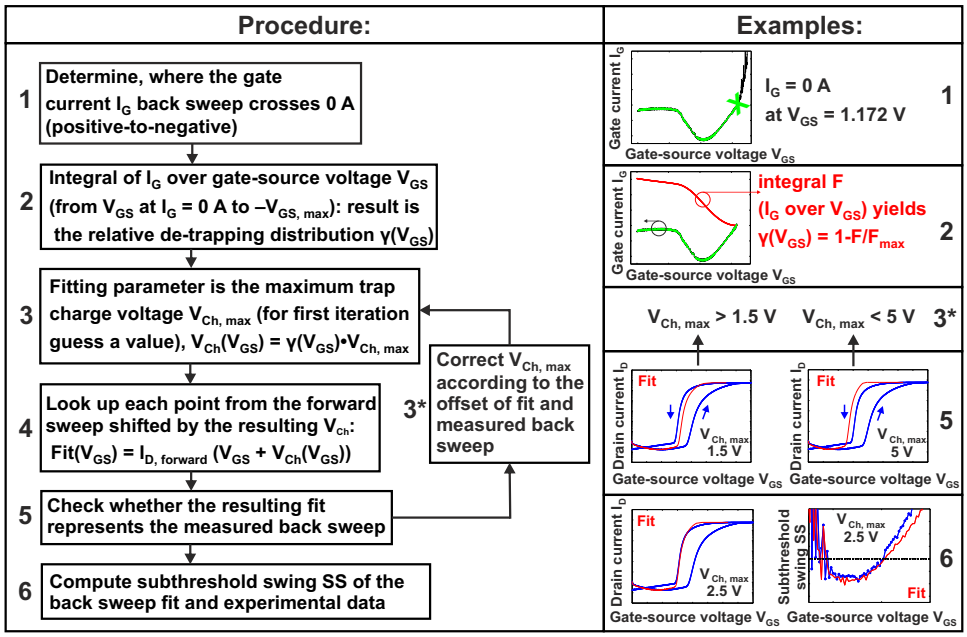

Fig. 5. Procedure for fitting the back sweep drain current I_D of a thin-film transistor using the forward sweep I_D as a reference and the back sweep gate current I_G for the relative de-trapping distribution.

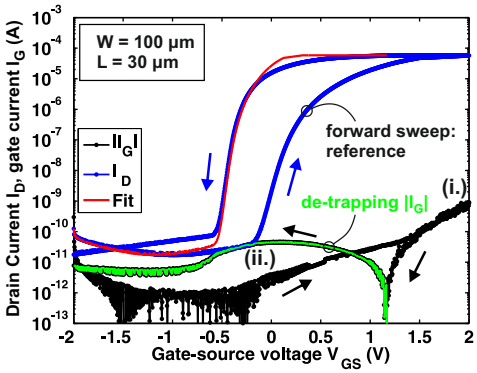

Fig. 6. Thin-film transistor transfer characteristic after fitting the back sweep drain current I_D using the forward sweep I_D as a reference and the gate current I_G for the relative trap charge distribution. (i.) and (ii.) denote the positive charge trapping and de-trapping, respectively.

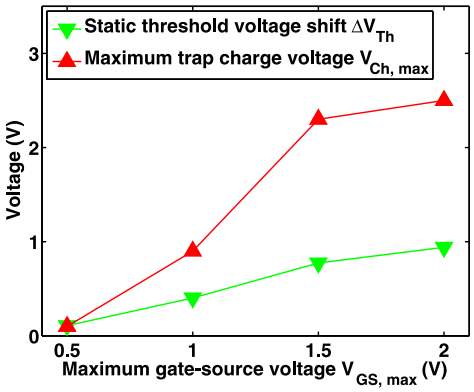

Fig. 7. Maximum fitted trap charge voltage $V_{Ch,max}$ and measured static threshold voltage shift ΔV_{Th} as a function of the maximum gate-source voltage $V_{GS,max}$.

where V_{DE} is the voltage over the gate dielectric and V_{FB} is the flat-band potential. From [35], we know that the subthreshold I_D can be approximated with $I_D \approx \exp(\beta \cdot \Psi_{sem})$ with $\beta = q/(k_B \cdot T)$, where q is the elemental electric charge, k_B is the Boltzmann constant and T is the temperature. The equation for the subthreshold slope S is given by

$$S = \frac{\partial(log_{10}(I_D))}{\partial V_{GS}}. \tag{2}$$

Consequently, the relationship between S and Ψ_{sem} is

$$S = \frac{\beta}{ln(10)} \cdot \frac{\partial \Psi_{sem}(V_{GS} + V_{Ch}(V_{GS}))}{\partial V_{GS}}. \tag{3}$$

In our case, Ψ_{sem} also depends on V_{Ch} which is a function of V_{GS}. With $\beta_0 = \frac{\beta}{\ln(10)}$, this leads to the following expression for S:

$$S = \beta_0 \cdot \frac{\partial \Psi_{sem}}{\partial(V_{GS} + V_{Ch}(V_{GS}))} \cdot \frac{\partial(V_{GS} + V_{Ch}(V_{GS}))}{\partial V_{GS}}. \tag{4}$$

The first part of this equation, declared as S_0, is identical to S for a standard FET [35] and the second part provides our amplification factor α_S. Therefore, (4) can be simplified to

$$S = S_0 \cdot \left(1 + \frac{\partial V_{Ch}(V_{GS})}{\partial V_{GS}}\right) = S_0 \cdot \alpha_S. \tag{5}$$

The final SS expression becomes

$$SS = S^{-1} = SS_0 \cdot \frac{1}{\alpha_S}. \tag{6}$$

Thus, we have found that α_S depends on the change rate of V_{Ch}.

In the following, we verify that our experimentally realized

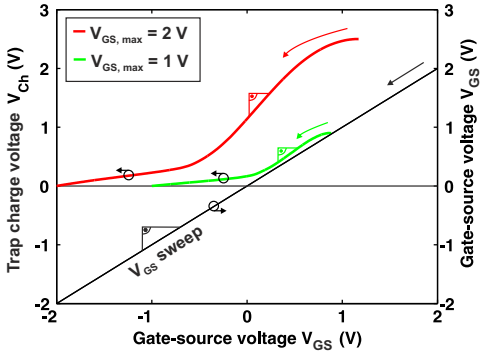

Fig. 8. Trap charge voltage V_{Ch} as a function of the gate-source voltage V_{GS} for two different maximum gate-source voltages $V_{GS,max}$. The V_{GS} sweep is given for comparison.

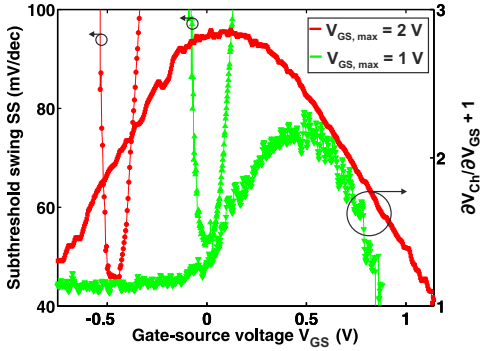

Fig. 9. $\partial V_{Ch}/\partial V_{GS}$ + 1, which constitutes the amplification factor α_S for $V_{GS} < V_{Th}$, as a function of the gate-source voltage V_{GS} for two different maximum gate-source voltages $V_{GS,max}$. The overlap of α_S with the subthreshold swing SS shows the effect on the switching behavior of the thin-film transistor.

TFT complies with the above described theoretical model and that the obtained α_S accurately describes the SS change in our devices. As a starting point, we plot V_{Ch}, that was obtained by the previously described fitting approach, as a function of V_{GS}. The resulting V_{Ch} for two different $V_{GS,max}$ is displayed in Fig. 8, while the marked slopes indicate the regions with the highest change rate. With the help of (5), the V_{Ch} vs. V_{GS} dependence can be numerically transformed into α_S (valid for $V_{GS} < V_{Th}$). The result is shown in Fig. 9 together with the experimentally obtained back sweep SS. Evidently, the magnitude of $\partial V_{Ch}/\partial V_{GS}$ + 1 (i.e. α_S for $V_{GS} < V_{Th}$) rises with a greater $V_{GS,max}$. Additionally, the V_{GS} positions for the maximum of $\partial V_{Ch}/\partial V_{GS}$ + 1 and the minimum SS approach each other for greater $V_{GS,max}$, which results in an increased impact of the charge de-trapping on the TFT switching. The shift of this de-trapping maximum towards negative V_{GS} indicates that the trap charge distribution extends into a greater depth within the gate dielectric. Our calculations, and especially the result shown in (6), are validated in Fig. 10. The forward sweep SS (not shown) is shifted by V_{Ch}, which corrects for the static impact of V_{Ch}. Then, the shifted forward sweep SS (blue) is divided by α_S (black). The results (red) match with the experimental back sweep SS (green) and hence confirm the validity of our modeling approach. The minimum forward sweep SS divided by α_S for different $V_{GS,max}$ is compared to the experimental back sweep SS in Fig. 11.

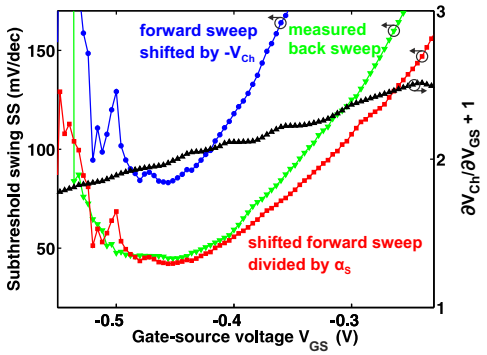

Fig. 10. Application of $\partial V_{Ch}/\partial V_{GS}$ + 1, which constitutes the amplification factor α_S for $V_{GS} < V_{Th}$, to the shifted forward sweep subthreshold swing SS showing the agreement of experimental and modeled back sweep SS.

V. Impedance-Voltage Measurements

The confirmation of the capacitive coupling of V_{Ch} to the FET channel lets us conclude that our experimentally investigated device stack contains NC components which cause the SS reduction. Consequently, we investigate their existence in impedance-voltage measurements. For that purpose, we compare Cu-Al_2O_3-IGZO metal-oxide-semiconductor (MOS) capacitors and Cu-Al_2O_3-Ti/Au/Ti metal-insulator-metal (MIM) capacitors. The resulting capacitance density, extracted with the parallel RC circuit model from the impedance measurement, and phase θ are displayed in Fig. 12(a) and Fig. 12(b), respectively. The MOS capacitor has the typical semiconductor capacitance transition from depletion to accumulation with a counter-clockwise hysteresis caused by the positive V_{Ch}.

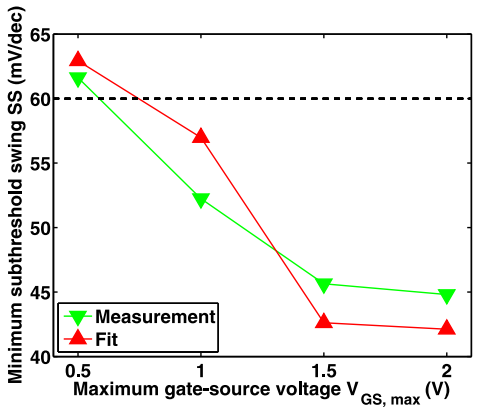

Fig. 11. Minimum subthreshold swing SS for different maximum gate-source voltages $V_{GS,max}$. The measured back sweep SS is compared to the fit which consists of the measured forward sweep SS divided by the amplification factor α_S.

Interestingly, the MIM capacitor shows NC (positive phase θ) at positive voltage, which occurs when the charge generation has a high rate and the tunneling current is large (see also I_G in Fig. 3(a)). This configuration appears to be similar to the NC reported in Schottky diodes under forward bias condition [17]–[19], which has mainly been observed at low frequencies [17], [18] and is related to charge carrier capture/emission processes

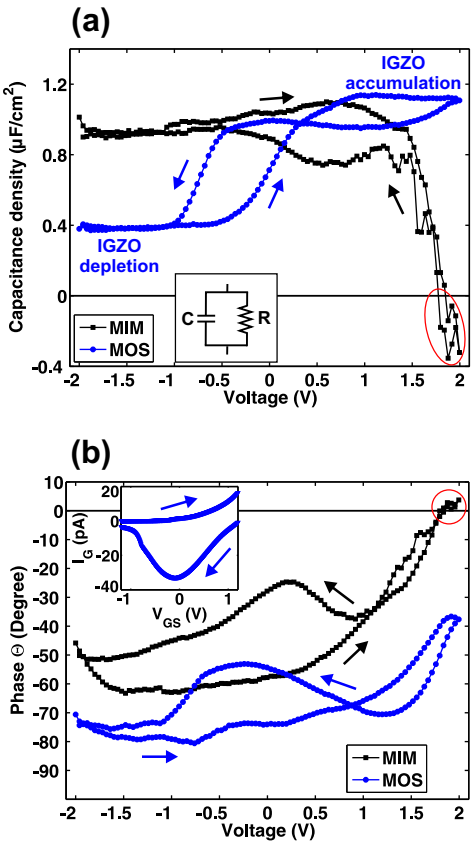

Fig. 12. Impedance-voltage measurement of a Cu-Al_2O_3-IGZO metal-oxide semiconductor (MOS) capacitor and a Cu-Al_2O_3-Ti/Au/Ti metal-insulator-metal (MIM) capacitor measured at a frequency of 1 Hz. (a) Capacitance density extracted with the parallel RC circuit model (inset). The MIM capacitor exhibits negative capacitance at positive voltage. (b) Phase θ, the phase of the MIM capacitor becomes positive at positive voltage and both devices have a phase peak in the back sweep. The phase peak of the MOS capacitor extends over the same voltage range as the negative gate current I_G peak in a thin-film transistor (see inset, where V_{GS} denotes the gate-source voltage).

at traps close to the metal-insulator interface [18], [19], [22]. These trap charging mechanisms, which are typically slow processes, can lead to a time delayed modulation of the dielectric tunnel barrier [23]. Hence, the trap charging current itself as well as a trap-related change in the tunneling transmission can both lead to a NC response, where the measured current lacks behind the applied voltage.

For the back sweep, θ of both structures rises when the charges are de-trapped, leading to a capacitance increase. The θ peak of the MOS capacitor appears in the same voltage range as the negative I_G (see inset, Fig. 12(b)) confirming the relation between the increase of θ and the de-trapping. The accompanied capacitance increase is an indirect sign of NC because the series connection of a positive and negative capacitance can result in an overall larger capacitance [27]. The co-existance of a capacitance rise and a SS reduction below 60 mV/dec for the MOS devices indicate such NC components in this material system. Concluding, these results suggest that the SS reduction is caused by an embedded/hidden NC that becomes active during charge exchange between the gate dielectric and the gate electrode.

VI. Conclusion and Outlook

In summary, we have found that charge exchange between the Cu gate electrode and the Al_2O_3 gate insulator has a strong impact on IGZO TFTs. In our experimental results, I_D shows counter-clockwise hysteresis and the SS reduces down to a minimum value of 46 mV/dec at room temperature. We mentioned in [32] that, in this device, the positive charge generation originates from impact ionization or multi-phonon ionization at positive voltage and the de-trapping is achieved through resonant tunneling. The latter, causing the SS reduction, appears to be promising for steep transistor switching. This mechanism can be further investigated in quantum well gate stacks where both trapping and de-trapping (from the gate) happens through resonant tunneling, which may lead to reduced hysteresis and steep SS in both sweep directions.
With our modeling, we have proven that the specifically defined amplification factor α_S applies to all FETs, where V_{Ch} capacitively couples to Ψ_{sem}. As a condition, a SS reduction requires that V_{Ch} changes in the same direction as V_{GS}, and consequently α_S becomes >1. Finally, the existence of NC in our material stack was shown by impedance-voltage measurements. In conclusion, the charge exchange between the gate electrode and the gate insulator provides a novel opportunity for the investigation of ultra-steep SS devices.

Acknowledgment

We would like to express our gratitude to Joakim Reuteler and Fabian Gramm for SEM, TEM and EDX imaging, and to Nuri Yazdani and Vanessa Wood for providing their CV test system. The work was funded by the Swiss National Science Foundation (SNSF) grant no. 2000021_149495/1.

References

[1] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, no. 7373, pp. 310–316, 2011.
[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.
[3] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, no. 7571, pp. 91–95, 2015.
[4] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "Impact ionization MOS (I-MOS)-Part I: device and circuit simulations," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 69–76, 2005.
[5] A. M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M. J. Declercq, P. Renaud, C. Hibert, P. Fluckiger, and G. A. Racine, "Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal-over-gate architecture," in *Proc. Int. Symp. on Quality Electronic Design*, San Jose, CA, USA, 2002, pp. 496–501.
[6] A. Jain and M. A. Alam, "Stability constraints define the minimum subthreshold swing of a negative capacitance field-effect transistor," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2235–2242, 2014.
[7] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.
[8] G. A. Salvatore, D. Bouvet, and A. M. Ionescu, "Demonstration of subthrehold swing smaller than 60mV/decade in Fe-FET with P (VDF-TrFE)/SiO 2 gate stack," in *IEEE Int. Electron Devices Meeting*. San Francisco, CA, USA: IEEE, 2008, pp. 1–4.
[9] S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry, and S. Datta, "Sub-kT/q switching in strong inversion in PbZr 0.52 Ti 0.48 O 3 gated negative capacitance FETs," *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 1, pp. 43–48, 2015.

[10] M. Keddam, Z. Stoynov, and H. Takenouti, "Impedance measurement on Pb/H 2 SO 4 batteries," *J. Appl. Electrochem.*, vol. 7, no. 6, pp. 539–544, 1977.
[11] A. K. Jonscher, "The physical origin of negative capacitance," *J. Chem. Soc., Faraday Trans. 2: Molecular and Chemical Physics*, vol. 82, no. 1, pp. 75–81, 1986.
[12] M. Ershov, H. Liu, L. Li, M. Buchanan, Z. Wasilewski, and A. K. Jonscher, "Negative capacitance effect in semiconductor devices," *IEEE Trans. Electron Devices*, vol. 45, no. 10, pp. 2196–2206, 1998.
[13] C. Zhu, L. Feng, C. Wang, H. Cong, G. Zhang, Z. Yang, and Z. Chen, "Negative capacitance in light-emitting devices," *Solid-State Electron.*, vol. 53, no. 3, pp. 324–328, 2009.
[14] J. Bisquert, G. Garcia-Belmonte, Á. Pitarch, and H. J. Bolink, "Negative capacitance caused by electron injection through interfacial states in organic light-emitting diodes," *Chem. Phys. Lett.*, vol. 422, no. 1, pp. 184–191, 2006.
[15] H. Okumoto and T. Tsutsui, "A source of negative capacitance in organic electronic devices observed by impedance spectroscopy: Self-heating effects," *Appl. Phys. Express*, vol. 7, no. 6, p. 061601, 2014.
[16] S.-T. Fu and M. Das, "Backgate-induced characteristics of ion-implanted GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 34, no. 6, pp. 1245–1252, 1987.
[17] C. Champness and W. Clark, "Anomalous inductive effect in selenium Schottky diodes," *Appl. Phys. Lett.*, vol. 56, no. 12, pp. 1104–1106, 1990.
[18] C. Wang, C. Zhu, G. Zhang, J. Shen, and L. Li, "Accurate electrical characterization of forward AC behavior of real semiconductor diode: giant negative capacitance and nonlinear interfacial layer," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1145–1148, 2003.
[19] X. Wu, E. Yang, and H. Evans, "Negative capacitance at metal-semiconductor interfaces," *J. Appl. Phys.*, vol. 68, no. 6, pp. 2845–2848, 1990.
[20] F. Lemmi and N. Johnson, "Negative capacitance in forward biased hydrogenated amorphous silicon p+-i-n+ diodes," *Appl. Phys. Lett.*, vol. 74, no. 2, pp. 251–253, 1999.
[21] T. Noguchi, M. Kitagawa, and I. Taniguchi, "Negative capacitance of silicon diode with deep level traps," *Jpn. J. Appl. Phys.*, vol. 19, no. 7, p. 1423, 1980.
[22] N. Chen, P. Wang, and J. Chen, "Low frequency negative capacitance behavior of molecular beam epitaxial GaAs n-low temperature-ip structure with low temperature layer grown at a low temperature," *Appl. Phys. Lett.*, vol. 72, no. 9, pp. 1081–1083, 1998.
[23] A. Perera, W. Shen, M. Ershov, H. Liu, M. Buchanan, and W. Schaff, "Negative capacitance of GaAs homojunction far-infrared detectors," *Appl. Phys. Lett.*, vol. 74, no. 21, pp. 3167–3169, 1999.
[24] E. Knapp and B. Ruhstaller, "Analysis of negative capacitance and self-heating in organic semiconductor devices," *J. Appl. Phys.*, vol. 117, no. 13, p. 135501, 2015.
[25] A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Pan, R. Ramesh, and S. Salahuddin, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Appl. Phys. Lett.*, vol. 99, no. 11, p. 113501, 2011.
[26] D. J. Appleby, N. K. Ponon, K. S. Kwa, B. Zou, P. K. Petrov, T. Wang, N. M. Alford, and A. ONeill, "Experimental observation of negative capacitance in ferroelectrics at room temperature," *Nano Lett.*, vol. 14, no. 7, pp. 3864–3868, 2014.
[27] W. Gao, A. Khan, X. Marti, C. Nelson, C. Serrao, J. Ravichandran, R. Ramesh, and S. Salahuddin, "Room-temperature negative capacitance in a ferroelectric–dielectric superlattice heterostructure," *Nano Lett.*, vol. 14, no. 10, pp. 5814–5819, 2014.
[28] P. McWhorter and P. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 48, no. 2, pp. 133–135, 1986.
[29] R. Schomer, P. Friedrichs, D. Peters, and D. Stephani, "Significantly improved performance of MOSFETs on silicon carbide using the 15R-SiC polytype," *IEEE Electron Device Lett.*, vol. 20, no. 5, pp. 241–244, 1999.
[30] A. Gangwar and B. Mazhari, "A thin-film transistor with high drain current induced by a trap-assisted electric double layer," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4776–4781, 2016.
[31] A. Ueda, S.-M. Jung, T. Mizutani, A. Kumar, T. Saraya, and T. Hiramoto, "Ultra-low voltage (0.1 V) operation of Vth self-adjusting MOSFET and SRAM cell," in *Symp. on VLSI Technology: Dig. Tech. Pap.* Honolulu, HI, USA: IEEE, 2014, pp. 1–2.
[32] A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G. A. Salvatore, and G. Tröster, "Positive charge trapping phenomenon in n-channel thin-film transistors with amorphous alumina gate insulators," *J. Appl. Phys.*, vol. 120, no. 24, p. 244501, 2016.
[33] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.
[34] R.-i. Yamada, J. Yugami, and M. Ohkura, "Charging and intrinsic-leakage current peaks in thin silicon-dioxide films," in *Symp. on VLSI Technology. Dig. of Tech. Paper*, Kyoto, Japan, 1997, pp. 147–148.
[35] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. John wiley & sons, 2007.

PLACE PHOTO HERE

Alwin Daus received the M.Sc. degree in electrical engineering from Braunschweig University of Technology, Braunschweig, Germany, in 2013. Since 2014, he has been pursuing the Ph.D. degree with the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. His current research interests include flexible thin-film transistors and the integration and study of novel gate materials.

PLACE PHOTO HERE

Christian Vogt (S'14) received the M.Sc. degree in electrical engineering and information technology from the Swiss Federal Institute of Technology (ETH) Zurich in 2013. Since 2013 he has been persuing the Ph.D. degree with the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. His current research interests include flexible electronics and applications for magnetic resonance imaging.

PLACE PHOTO HERE

Niko Münzenrieder (S'11-M'14) received a diploma in physics from the Technical University Munich in 2008, and a Ph.D. in electrical engineering from the Swiss Federal Institute of Technology Zurich in 2013. Currently, he is a Lecturer at the University of Sussex working on flexible and stretchable thin-film electronics.

PLACE PHOTO HERE

Luisa Petti (S'12-M'16) received the M.Sc. degree in electronic engineering from Politecnico di Milano in 2011, and the Ph.D. degree in electrical engineering and information technology from Swiss Federal Institute of Technology (ETH) Zurich in 2016. Her current research interests are the development, fabrication, and characterization of flexible thin-film devices and circuits based on metal oxide semiconductors.

PLACE PHOTO HERE

Stefan Knobelspies received his B.Sc. and M.Sc. degrees in microsystems engineering from the Albert-Ludwigs-University Freiburg, Germany in 2011 and 2015, respectively. He joined the Institute for Electronics, Swiss Federal Institute of Technology (ETH), Zurich, Switzerland in 2015, where he is currently working towards the Ph.D. degree. His research is focused on thin-film electronics and devices on flexible substrates.

PLACE PHOTO HERE

Giuseppe Cantarella received the M.Sc. degree in electronic engineering from Polytechnic of Turin, Turin, Italy, in 2013. Since 2013, he has been pursuing the Ph.D. degree with the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. His current research interests include flexible electronics.

PLACE PHOTO HERE

Giovanni A. Salvatore received the M.Sc. from Polytechnic of Turin and the PhD from EPFL in electronic engineering in 2006 and in 2011, respectively. He joined the Wearable Computing Lab at ETHZ in 2011. He works on materials, devices and circuits for flexible and textile electronics.

PLACE PHOTO HERE

Gerhard Tröster has been a full professor of electronics with the Swiss Federal Institute of Technology Zurich, Zurich, Switzerland, since 1993. His current research interests include signal processing, wireless sensor networks, wearable computing, smart textiles applying flexible, and organic electronics.